SEMICONDUCTOR LEADFRAMES COMPRISING SILVER PLATING

FIELD OF THE INVENTION

The present invention is related in general to the field of semiconductor devices and processes and more specifically to the materials and fabrication of leadframes for integrated circuit devices.

DESCRIPTION OF THE RELATED ART

The leadframe for semiconductor devices was invented (US Patents # 3,716,764 and # 4,034,027) to serve several needs of semiconductor devices and their operation simultaneously: First of all, the leadframe provides a stable support pad for firmly positioning the semiconductor chip, usually an integrated circuit (IC) chip. Since the leadframe including the pads is made of electrically conductive material, the pad may be biased, when needed, to any electrical potential required by the network involving the semiconductor device, especially the ground potential.

Secondly, the leadframe offers a plurality of conductive segments to bring various electrical conductors into close proximity of the chip. The remaining gap between the ("inner") tip of the segments and the conductor pads on the IC surface are typically bridged by thin metallic wires, individually bonded to the IC contact pads and the leadframe segments. Obviously, the technique of wire bonding implies that reliable welds can be formed at the (inner) segment tips.

Thirdly, the ends of the lead segment remote from the IC chip ("outer" tips) need to be electrically and mechanically connected to "other parts" or the "outside world", for instance to assembly printed circuit boards. In the overwhelming majority of electronic applications, this attachment is performed by soldering. Obviously, the technique of soldering implies that reliable wetting and solder contact can be performed at the (outer) segment tips.

It has been common practice to manufacture single piece leadframes from thin (about 120 to 250 µm) sheets of metal. For reasons of easy manufacturing, the commonly selected starting metals are copper, copper alloys, iron-nickel alloys for instance the so-called "Alloy 42"), and invar. The desired shape of the leadframe is etched or stamped from the original sheet. In this manner, an individual segment of the leadframe takes the form of a thin metallic strip with its particular geometric shape determined by the design. For most purposes, the length of a typical segment is considerably longer than its width.

In the European patent # 0 335 608 B1, issued 14 June 1995 (Abbott, "Leadframe with Reduced Corrosion"), a palladium-plated leadframe is introduced which is not subject to corrosion due to galvanic potential forces aiding the migration of the base metal ions to the top surface where they will form corrosion products. The patent describes a sequence of layers consisting of nickel (over the base metal), palladium/nickel alloy, nickel, and palladium (outermost). This technology has been widely accepted by the semiconductor industry.

After assembly on the leadframe, most ICs are encapsulated, commonly by plastic material in a molding

process. It is essential that the molding compound, usually an epoxy-based thermoset compound, has good adhesion to the leadframe and the device parts it encapsulates. Palladium, described above as the outermost layer of the leadframe, offers excellent adhesion to molding compounds.

Nickel/palladium plated leadframes are used because of their low total cost of ownership, primarily a result of eliminating post-mold solder plating. However, some customers, for instance automotive manufacturers and telephone central switching offices, require solder plated external leads, typically because of burn-in, accelerated testing or environmental conditions. Unfortunately, using a fully nickel/palladium plated leadframe precludes solder plating after molding because the tin in the solder reacts with the palladium to form a tin-palladium intermetallic that is not solderable.

If solder dipping is used after molding, the palladium will dissolve into the solder and the nickel is then solderable. However, solder dipping is not practical for devices with fine-pitch leadframes because of solder bridging.

The price of palladium climbed in the last decade from about one third of the gold price to approximately twice the gold price. Cost reduction pressures in semiconductor manufacturing have initiated efforts to reduce the thickness of the palladium layers employed to about one third of its previous thickness. At this thinness, palladium does not prevent oxidation of the underlying nickel which will inhibit its solderability.

In U.S. Patent Application # 60/138,070, filed on 8 June 1999 (Abbott, "Palladium-Spot Leadframes for Solder

Plated Semiconductor Devices and Method of Fabrication", TI-28784), to which the present invention is related, a fabrication process for palladium layers of reduced thickness is described (combined with a process for post-mold plating solder layers). However, the solders of the leadframe still contain lead, while the recent trend in the semiconductor industry, driven by environmental concerns, aims at lead-free solders.

In U.S. Patent Application # 60/214,314, filed on 27 June 2000 (Abbott, "Semiconductor Leadframes Plated with Lead-free Solder and Minimum Palladium", TI-29878), to which the present invention is related, a fabrication for selectively plated lead-free solder layers is described (combined with a process for selective thin palladium layers). However, for many applications, the solder attachment temperature should preferably be lower than the melting temperature of binary lead-free alloys. Further, it is problematic to produce reliable wire bond stitches to extremely thin palladium layers.

An urgent need has therefore arisen for a low-cost, reliable mass production method for a leadframe combining the advantages of good bondability, adhesion capability to molding compounds, and the application of pre-plated lead-free solders. Palladium layers should have minimal thickness. The leadframe and its method of fabrication should be flexible enough to be applied for different semiconductor product families and a wide spectrum of design and assembly variations, and should achieve improvements toward the goals of improved process yields and device reliability. Preferably, these innovations should be accomplished using the installed equipment base

so that no investment in new manufacturing machines is needed.

SUMMARY OF THE INVENTION

According to the present invention for a semiconductor integrated circuit (IC) leadframe, a base metal with a plated layer of nickel fully covering the base metal has a plated layer of lead-free solder on the nickel layer selectively covering areas of the leadframe intended for attachment to other parts; a plated layer of palladium on the nickel layer selectively covering areas of the leadframe intended for bonding wire attachment; and a plated layer of silver on both the palladium and the solder layers thin enough so that the portion of the silver on the solder is completely dissolved into the solder upon heating.

The present invention is related to high density ICs, especially those having high numbers of inputs/outputs, or contact pads, and also to devices in packages requiring surface mount in printed circuit board assembly. These ICs can be found in many semiconductor device families such as standard linear and logic products, digital signal processors, microprocessors, digital and analog devices, and both large and small area chip categories. The invention represents a significant cost reduction and enhances environmental protection and assembly flexibility of semiconductor packages, especially the plastic molded packages, compared to the conventional copper-based solder-plated leadframes.

It is an aspect of the present invention to provide a technology for enabling solder package leads with pre-plated lead-free solder of low reflow temperature, while maintaining a palladium layer in the localized areas intended for wire bonding, where excellent bondability is

maintained in spite of extreme palladium thinness. These goals are reached by depositing over the leadframe an outermost layer of silver which is thin enough so that its portion over the solder is completely dissolved into the solder upon heating.

Another aspect of the invention is to provide the lead-free solder such that it dissolves in tin-rich solder paste or solder wave when its reflow temperature is higher than semiconductor assembly temperatures, and that it does not form tin or silver whiskers on the outside of the package.

Another aspect of the invention is to reach these goals with a low-cost manufacturing method without the cost of equipment changes and new capital investment, by using the installed fabrication equipment base.

Another aspect of the invention is to produce leadframes so that established wire bonding processes can continue unchanged, due to excellent bondability to silver, and that established board attachment process can continue unchanged, due to excellent solderability.

Another aspect of the invention is to introduce a palladium spot plating technology with provides loose tolerance for the spot boundaries, thus simplifying leadframe manufacturing and lowering fabrication cost.

These aspects have been achieved by the teachings of the invention concerning deposition and masking methods suitable for mass production. Various modifications of leadframe preparations have been successfully employed.

In the preferred embodiment of the invention, a plated layer of nickel is fully covering the leadframe base material. A plated layer of lead-free solder is plated onto the nickel layer so that it covers selectively

leadframe areas intended for parts attachment, especially board assembly. A layer of palladium is then plated onto the nickel layer so that it covers selectively the leadframe areas intended for bonding wire attachment. Finally, an outermost layer of silver is food plated over the whole leadframe. It has a thinness so that its portion on the solder layer is dissolved into the solder during the temperature and time excursions in the processes of chip attaching and curing, wire bonding, and molding and curing.

Leadframes prepared according to the invention can be successfully used in surface mount technologies based on bending the package lead segments.

The technical advances represented by the invention, as well as the aspects thereof, will become apparent from the following description of the preferred embodiments of the invention, when considered in conjunction with the accompanying drawings and the novel features set forth in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a schematic and simplified cross sectional view of a leadframe with base metal and first plated layer.

FIG. 2 is a schematic and simplified cross sectional view of a leadframe after the plating step for lead-free solder according to the invention.

FIG. 3 is a simplified top view of an example of a leadframe unit for semiconductor devices, delineating the masking needed in the lead-free solder plating fabrication method according to the invention.

FIG. 4 is a schematic and simplified cross sectional view of a leadframe after the plating step for wire bonding enhancement according to the invention.

FIG. 5 is a simplified top view of an example of a leadframe unit for semiconductor devices, delineating the masking needed in the plating fabrication method for wire bonding enhancement according to the invention.

FIG. 6 is a schematic and simplified cross sectional view of a leadframe after the plating step for silver layer deposition according to the invention.

FIG. 7 is a schematic and simplified cross sectional view of a packaged semiconductor device having a leadframe according to the invention, lead-free solder assembled on a substrate.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention is related to U.S. Patent Applications # 60/214,314, filed on 27 June 2000 (Abbott, "Semiconductor Leadframes Plated with Lead-free Solder and Minimum Palladion", TI-29878) and # 60/138,070, filed on 8 June 1999 (Abbott, "Palladium-Spot Leadframes for Solder Plated Semiconductor Devices and Method of Fabrication", TI-28784).

The present invention is related to the assembly of semiconductor ICs on leadframes, including wire bonding interconnection, and their final encapsulation, the sequential construction of these leadframes using deposited layers of various metals, and the environmentally friendly process of reliable attachment of the devices to substrates using lead-free solder.

The invention reduces the cost of leadframes while the leadframe functions are maximized. The invention best applies to any leadframe and any substrate used in semiconductor technology which exhibit the following design features: Usually, a chip mount pad for support of the IC chip surrounded by lead segments, each having a first end in proximity of the chip pad, and a second end remote from the chip pad. The invention thus applies to semiconductor package types such as PDIPs, SOICs, QFPs, SSOPs, TQFPs, TSSOPs and TVSOPs.

As defined herein, the starting material of the leadframe is called the "base metal", indicating the type of metal. Consequently, the term "base metal" is not to be construed in an electrochemical sense (as in opposition to 'noble metal') or in a structural sense. The base metal of leadframes is typically copper or copper alloys. Other

choices comprise brass, aluminum, iron-nickel alloys ("Alloy 42"), and invar.

Leadframe segments have to satisfy five needs in semiconductor assembly:

1) Leadframes have to comprise segment ends remote from the chip mount pad ("outer segments") for solder attachment to other parts;
2) leadframes have to comprise segment ends near the chip mount pad ("inner segments") for bond attachments to wire interconnections;
3) leadframes have to comprise outer segments ductile for forming and bending the segments;
4) leadframe surfaces have to comprise adhesion to molding compounds; and
5) leadframe segments have to comprise insensitivity to corrosion.

According to the teachings of this invention, Need 1) is satisfied by depositing a layer of nickel, fully covering the leadframe base metal, and then selectively preplating a layer of solder onto the nickel layer only onto those leadframe areas which are intended for parts attachment. Solderability is enhanced by depositing a layer of silver over the solder in such thinness that the silver completely dissolved into the solder when the device undergoes processes at elevated temperatures for a period of time. Complete silver dissolution avoids any free silver for dendrite formation. It further establishes a solder of tertiary alloy with lower reflow temperature compared to the binary alloy without silver.

The invention satisfies Need 2) by first plating the nickel layer, fully covering the leadframe base metal as outlined above, then plating a thin layer of palladium onto

the nickel layer, selectively covering areas of the leadframe which are intended for bonding wire attachment (and chip attachment) and finally plating a silver layer over the thin palladium. For palladium, a thin layer is sufficient for reliable bonding wire attachment (stitch bonds, ball bonds, or wedge bonds), since the silver is known to have excellent characteristics for wire bonding.

The invention satisfies Need 3) by the selection of thickness and structure of the nickel layer employed to fulfill need 1). Thickness and deposition method of the nickel layer have to be selected such that the layer insures ductility and enables the bending and forming of the outer lead segments.

The invention satisfies Need 4) by the choice of the noble metal layer employed to fulfill need 2); a practical selection is silver with its excellent adhesion to thermoset molding compounds and other encapsulation materials; a thin layer of gold would be another option.

The invention satisfies Need 5) by the sequence of layers deposited over the copper base: Nickel and solder.

FIG. 1 is a schematic and simplified cross section of a leadframe portion, generally designated 100, and shows the chip mount pad 101 and a plurality of lead segments 102. The leadframe is made of a base metal 103 fully covered with a plated layer 104. The base metal usually is copper or copper alloy, but may also be aluminum, brass, an iron-nickel alloy, or invar. The copper or copper alloy base sheet 103 has a preferred thickness in the range from 100 to 300 µm; thinner sheets are possible. The ductility in this thickness range provides the 5 to 15 % elongation needed in the segment bending and forming operation. The leadframe is stamped or etched from the starting metal

sheet. The plated nickel layer has a preferred thickness is the range from about 0.5 to 3.0 μm.

In the plating process, the stamped or etched leadframe is first immersed in an alkaline preclean solution at 20 to 90 °C for few seconds up to 3 minutes. Both alkaline soak cleaning and alkaline electrocleaning are employed. Oils, grease, soil, dirt and other contamination are thereby removed.

After rinsing, the leadframe is next immersed in an acid activation bath at room temperature for few seconds up to 5 minutes. The bath consists of a solution of sulfuric acid, hydrochloric acid, or other acid solution, preferably at about 30 to 60 g/l concentration. This solution removes copper oxide and leaves the metallic copper oxide surface in an activated state, ready to accept the deposition of metallic nickel.

Next, the leadframe is immersed in a first nickel plating solution to receive the deposition onto the copper base material of a nickel strike in the thickness range of about 0.02 to 0.13 μm. This first nickel layer fully encases the copper base metal and thus keeps the subsequent main nickel bath free from copper and copper compounds.

Next, the leadframe is immersed in a second nickel plating solution to receive the deposition onto the first nickel layer of an additional nickel layer in the thickness range of about 0.45 to 2.0 μm. The total thickness range of layer 104 is approximately 0.5 to 3.0 μm. This nickel layer has to be ductile for the leadframe segment bending and forming process. Further, the nickel surface has to be wettable in the soldering process, so that solder alloys or conductive adhesives can be used successfully.

In FIG. 2, a layer 206 of solder is plated selectively onto the flood plated layer 104 of nickel over the leadframe base material 103. The solder layer has a thickness in the range from about 0.7 to 9 µm. As this range shows, the solder layer can be relatively thin compared to conventional solder thickness ranges; the reason is the additional silver layer discussed below. The solder plated portions cover the areas of the leadframe intended for board attach or other parts attachment, specifically the second ends of the lead segments, remote from the chip mount pad. The boundary of the solder plated portion is designated 206a in FIG. 2. It is an advantage of the invention that boundary 206a may have loose tolerances.

It is of important to the present invention that

* the solder is lead-free;
* the solder is deposited as a pre-plated layer, i.e., applied to the leadframe before the start of chip assembly;
* the solder may have a reflow temperature higher than IC assembly temperatures, including wire bonding and package molding (it may be lowered by the addition of silver, see below);
* the solder is able to dissolve into the solder flux or wave during device board attach and
* the solder avoids tin whisker growth.

The electronic industry has been searching for a substitute for the customary lead in the solder for several years. Recent reviews on the status of this search are, for instance, given by the National Center for Manufacturing Sciences, "NCMS Lead-free Solder Project", Surface Mount Technology, vol. 14, no. 2, pp. 73 - 80,

2000; and by J. S. Hwang, Z. Guo, and H. Koenigsmann, "High-strength and High-fatigue-resistant Lead-free Solder", Surface Mount Techn., vol. 14, no. 3, pp. 55 - 60, 2000.

Various binary and tertiary alloys have been discussed. For example, U.S. Patent # 5,985,212, issued on 16 Nov. 1999 (Hwang et al., "High Strength Lead-free Solder Materials"), recommends at least 75 weight % tin, between about 0.01 and 9.5 weight % Cu, between about 0.01 and 5.0 weight % gallium, and between about > 0 and 6 % indium.

For the intent of the present invention, the solder layer may comprise materials selected from a group consisting of tin, binary tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tertiary alloys (also containing gallium), and conductive adhesive compounds. A preferred easy-to-plate solder alloy is a binary tin and copper alloy; a tin and silver alloy is another preferred solder. The composition is to be optimized to bring the reflow temperature above the temperatures seen at the various assembly steps (chip attach, wire bonding, molding, curing) which vary from device to device. For example, if 270 °C is the target, 2.5 weight % copper is appropriate in the tin/copper alloy; if 300 °C is the target, 5.0 weight % copper is appropriate. The tin/copper, or tin/silver alloy does not need to melt, but will rather dissolve into the solder paste or wave, offering good wetability of the underlying nickel. As discussed below, the solder reflow temperature may be lowered due to the addition of silver, in which case the solder may reflow in the conventional sense without dissolution in the soldering media.

It is an important aspect of the present invention to deposit the solder alloy layer selectively onto the

leadframe using an inexpensive, temporary masking step, which leaves only those leadframe portions exposed which are intended to receive the solder layer. An example of the extent of such masking is depicted in FIG. 3, which shows a single leadframe unit from a continuous strip, for a typical semiconductor Quad Flat Pak device. The temporarily masked parts of the leadframe unit are shaded and the exposed parts are unshaded. The exposed parts include the second ends 34 of the plurality of lead segments 33, remote from chip mount pad 35.

As defined herein, each lead segment 33 has a first end 32 near the chip mount pad 35 and a second end 34 remote from chip mount pad 35. In the example of FIG. 3, the leadframe unit has 84 lead segments 33, since it is designed for a plastic 84-lead Quad Flat Pak chip carrier.

Further, the temporarily masked portions of the leadframe include carrier rails 30, outer leadframe 31, portions of the plurality of support members 36, which extend from carrier rail 30 toward chip mount pad 35, and dam bar 37. In the example of FIG. 3, the device has 4 support members 36.

There are several methods to selectively deposit metals from solution onto a continuous strip. For high volume production of leadframes, continuous strip or reel-to-reel plating is advantageous and common practice. Based on the loose tolerance acceptable for the boundaries of the solder plating on the second ends of the lead segments, the preferred deposition method for the present invention is the so-called "wheel system". The process steps are as follows.

** WHEEL SYSTEM

* Material is moved over a large diameter wheel

with apertures in it to allow solution flow to material;

* apertures define the locations for plating; index pins engage the pilot holes (designated 38 in FIG. 3) in the leadframe;
* backing belt is used to hold material on wheel and mask backside of material;
* anode is stationary inside wheel.

Advantages: Fast, material never stops for selective plating; no timing issues; pumps, rectifiers, and drive system are on continuously; low cost because system is mechanically uncomplicated.

Disadvantages: Loose plating boundaries, poor spot location, and potential bleedout are not critical issues for the present invention.

A more precise, but also more costly and slower selective plating technique is the step-and-repeat process.

** STEP AND REPEAT

* Leadframe material is stopped in selective plating head;
* rubber mask system clamps on material;
* plating solution is jetted at material;
* current is applied;
* current is shut off;
* solution is shut off;
* head opens;
* material moves.

Advantages: Very sharp plating spot with excellent edge definition; very good spot location capability when used with index holes, pins and feedback vision system.

Disadvantages: Slow; material must stop during selective plating; expensive equipment to buy and maintain; timing issues; lots of moving parts.

The schematic cross section of a leadframe in FIG. 4 depicts the thin palladium layer 405, plated on the area of chip pad 401 and the first ends 403 of segment 402 near the chip pad. The deposited layer 405 comprises an electroplated palladium layer in the thickness range of about 5 to 250 nm. Due to the high price of palladium, the thinnest layers are preferred; excellent bondability is insured by the addition of the silver layer (see below). Another choice as noble metal would be rhodium. The area portion 403 of the plurality of lead segments is determined by the technical requirement of the intended wire bonding attachment. In the schematic example of FIG. 4, layer 405 terminates at boundary 405a. It is an advantage of the invention that boundary 405a may have loose tolerances.

It is an important aspect of the present invention to deposit the palladium layer selectively onto the leadframe by using an inexpensive masking step, analogous to the solder plating process described in FIGs. 2 and 3. The selective characteristic of the palladium deposition is achieved by a temporary masking step, which leaves only those leadframe portions exposed which are intended to receive the palladium layer. An example of the extent of such masking is depicted in FIG. 5, which shows a single leadframe unit from a continuous strip, for a typical semiconductor Quad Flat Pak device analogous to FIG. 3. The temporarily masked parts of the leadframe unit are shaded and the exposed parts are unshaded. The exposed parts include the first ends 52 of the plurality of leadframe leads 53, the chip pad 55, and the portions 56 of

the support members of the chip pad. These first ends are positioned near chip pad 55. In FIG. 5, the first ends 52 surround the periphery of chip pad 55, but are separated from the pad by the gap which will be bridged by the bonding wires.

The methods to deposit palladium are analogous to the methods for depositing solder described above. For many practical cases, the "wheel system method" produces satisfactory precision while featuring desirable low cost.

The schematic cross section of the leadframe in FIG. 6 is analogous to the cross sections in FIGs. 1, 2 and 4. FIG. 6 shows the addition of the flood plated silver layer 601, encapsulating the exposed leadframe areas. The silver layer 601 has a thickness in the range from about 20 to 2500 nm; the preferred thickness range is from about 1200 to 1500 nm. Silver layer portion 601a is deposited on the solder layer 206. It is essential for the present invention that the silver layer 601 is thin enough so that silver layer portion 601a can be completely dissolved into the solder layer 206 upon exposure to elevated temperatures and extended times in the various assembly processes. These processes include chip attaching, curing of attach material, wire bonding, molding, curing of mold material. For example, during wire bonding, temperatures may reach as high as 250 °C for several minutes; during mold compound curing, 175 °C may be maintained for 6 hours. After dissolution into the solder layer, no free silver is left for any dendrite growth.

An example of formed outer leads of a finished molded package is illustrated in FIG. 7. In the schematic cross section of FIG. 7, the copper or copper alloy leadframe 701 of the invention is shown as applied in the

assembly of a semiconductor package generally designated 700. Leadframe 701 has a chip mount pad 702 onto which an IC chip 703 is attached using adhesive material 704 (typically an epoxy or polyimide which has to undergo polymerization). Leadframe 701 further has a plurality of lead segments 705. These lead segments have a first end 705a near the chip mount pad 702 and their second end 705b remote from mount pad 702.

As shown in FIG. 7 schematically, leadframe 701 comprises base 706 made of copper or copper alloy. On the surface of this copper is a sequence of layers, described in detail in FIGs. 1, 2, 4 and 6. Closest to the copper is a first layer 707 of nickel. This layer is followed by a spot-plated layer 708 of palladium, and a spot-plated layer 709 of solder. Outermost is the food plated silver layer 720. The composite solder layer is incorporated into the meniscus of the bulk solder 710 in the process of surface mounting device 700 onto a substrate or board.

In FIG. 7, bonding wires 711 have stitches 712 welded to the palladium and silver surface 708 of the first ends 705a of leadframe segments 705. The bonding wires are selected from a group consisting of gold, copper, aluminum, and alloys thereof. Any of these metals provide reliable welds to the layered leadframes of the invention.

As shown in FIG. 7, the second ends 705b of segments 705 are suitable for bending and forming due to the ductility of the copper base and the plated nickel layer. In general, copper leads plated with the tin/copper alloy of the invention have better trim/form performance than leads plated with the traditional lead/tin alloy due to improved ductility. Using this malleable characteristic, segments 705 may be formed in any shape required for

surface mounting or any other technique of board attach of the semiconductor devices. The bending of the segments does not diminish the corrosion protection of the second segment ends 705b. For example, FIG. 7 indicates a so-called "gull wing shape" of segments 705. This shape is widely used for IC packages in the so-called "small outline" configuration, as illustrated in FIG. 7.

The solder spot-plated copper leadframe, with the addition of the dissolved silver layer of the invention, provides for easy and reliable solder attachment to boards or other parts of the formed leadframe segments. In FIG. 7, solder attach material 710 comprises a solder paste or wave. As pointed out above, this paste may dissolve the plated tin/copper layer including the dissolved silver (indicated by the dashed lines in FIG. 7), resulting in good wetting characteristics to the plated nickel surface of the copper leadframe.

In FIG. 7, molding compound 713 encapsulates the mounted chip 703, bonding wires 711 and the first ends 705a of the lead segments 705. The second, remote ends 705b of the segments are not included in the molded package; they remain exposed for solder attachment. Typically, the encapsulation material 713 is selected from a group consisting of epoxy-based molding compounds suitable for adhesion to the leadframe surfaces. For the outermost silver plating, good adhesion characteristics to molding compounds can be achieved, preventing package delamination, moisture ingress and corrosion.

In regard to corrosion, it should be pointed out that copper creep corrosion is a function of the nobility of the exposed surface. In the present invention, the surface of the leadframe has nickel, nickel oxide,

tin/copper and silver on it. This will prevent copper creep corrosion as compared to a surface with pure palladium, and the performance in the mixed flowing gas corrosion tests is accordingly better.

OTHER EMBODIMENTS

While this invention has been described in reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art upon reference to the description. As an example, the material of the semiconductor chip may comprise silicon, silicon germanium, gallium arsenide, or any other semiconductor material used in manufacturing. As another example, the designs, cover areas and fabrication methods of the solder layer and of the palladium layer may be modified to suit specific leadframe or substrate needs.

As another example, the thickness of the silver plated layer can be adjusted to the temperatures and times employed in the process steps of device assembly in order to obtain optimum solder attachment and wire bonding results. As another example, the silver layer may be deposited not in a flood-plating process, but by using masks similar to the ones described in FIGs. 3 and 5, whereby the silver will not be deposited on the outer lead segments in the neighborhood just outside the molded package.

It is therefore intended that the appended claims encompass any such modifications or embodiments.